17/Appeal Brief Timely 6/6/03

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Mary V. Carter
Printed name of person mailing paper or fee

Mary V. Carter
Signature of person mailing paper or fee

Inventor(s):	**Frank Hui, Yifeng Yan, and Allen Yen**
Case:	**3-6-16**
Serial No.:	**09/653,295**
Filing Date:	**8/31/00**
Examiner:	**Nguyen, Cuong** Group Art Unit: **2815**
Title:	**Stacked Structure for Parallel Capacitors and Method of Fabrication**

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D. C. 20231

APPEAL BRIEF

Appellants hereby appeal the Examiner's rejections in the Final Office Action mailed 8/26/02. Three copies of this brief are transmitted herewith.

1. IDENTIFICATION OF THE REAL PARTY IN INTEREST

The real party in interest for the above-identified application is Agere Systems Inc. which is the assignee of record for the application.

2. IDENTIFICATION OF RELATED APPEALS OR INTERFERENCES

To the best of appellant's knowledge, there are no appeals or interferences that will be directly affected by or will have a bearing on the decision on appeal.

3. STATUS OF THE CLAIMS

Claims 1 – 10 are pending. Claims 7-10 have been withdrawn, but not cancelled, under a restriction requirement traversed by applicants. A petition to over rule the restriction requirement made final by the examiner is now pending.

Claims 1-6 have been examined and are the subject of this appeal. Claim 1 was amended during prosecution to fully distinguish over a rejection under Section 103(a) based on the examiner's combination of Arai ('804) in view of Watanabe ('490), which rejection is withdrawn.

A copy of the claims as amended is attached hereto as Appendix A. Appellants respectfully appeal the final rejection of claims 1-6.

4. STATUS OF THE AMENDMENTS

No amendments were made to the claims after final rejection.

5. BACKGROUND

Monolithic integrated circuits, commonly referred to as integrated circuits or chips, are well known devices that include a plurality of circuit elements formed on a common body of semiconductor material. See, for example, U.S. 3,541,357 (appended to this brief as Attachment I), filed April 29, 1968, which so defines monolithic integrated circuits at Col. 1, lines 25 – 33. The integration of capacitor structures and transistors on these devices has long been the subject of development efforts in order to increase the density, functionality and performance of electronic circuitry. See, for example, U.S. 4,245,231 "Combination Capacitor and Transistor Structure for Use in Monolithic Circuits" (appended to this brief as Attachment II). Generally, formation of capacitors in monolithic integrated circuits is well understood to mean fabrication of capacitor structures on the same common body of semiconductor material as other interconnected devices, e.g., transistors, to make an integrated circuit.

It is well known that inclusion of passive device structures such as capacitors in semiconductor integrated circuits can consume significant area. In the past, capacitance values have been increased without proportionately increasing the area consumed on an integrated circuit by forming multiple capacitors on separate metal levels and then connecting them in parallel. That is, capacitors have been formed in the various levels of interconnect overlying the semiconductor body. Recognizing that, as the dielectric thickness decreases, the capacitance increases, further reductions in layout areas may be considered primarily a function of material selection. Actually, efforts to reduce the physical size of a capacitor network are limited by several factors, including the required area of the pairs of capacitor plates, the characteristics of the intervening dielectric and the spacing between plates.

6. SUMMARY OF THE INVENTION

Most generally, the invention is directed to a monolithic integrated circuit comprising a stack of alternating conductive and insulative layers of the type used to form a capacitor structure. The embodiment shown in Figure 9 of the application (appended to this brief as Attachment III) is exemplary, and reference numerals corresponding to the device shown in this figure are now used for purposes of illustrating application of the invention. Above a semiconductor body (not

illustrated) a first level of interconnect conductor includes a metal runner 123. A second level of interconnect conductor (formed above the first level) includes metal runners 120 and 125. In this example the runners 120, 123 and 125 extend along the plane of the paper in a horizontal direction. The capacitor stack is formed between the first and second levels of interconnect conductor, e.g., between the lower runner 123 and the upper runners 120, 125. The stack comprises five conductor layers 122 sequentially formed with intervening dielectric layers 124 positioned between pairs of the layers 122 to provide capacitor dielectrics. Connections to individual layers 122 are made through via portions 126 and the runners 120, 123 and 125 to configure four capacitors connected in parallel. According to claim 1, the stack includes at least:

> a first conductive layer,
> a first insulator layer formed over the first conductive layer,
> a second conductive layer formed over the first insulative layer,
> a second insulator layer formed over the second conductive layer, and
> a third conductive layer formed over the second insulative layer,
> with the first and third conductive layers commonly connected.

Referring to the left half of Figure 9, it will be apparent when the layers 122 are sequentially numbered 1 through 5 (from bottom to top), that the first, third and fifth conductive layers are commonly connected by a combination of the runners 120 and 123 and three of the via portions 126.

7. ISSUES

The issues on appeal are (a) whether claims 1-3 and 5-6 are patentable over the combination of Saia et al. (U.S. Patent No. 5,736,448) in view of Watanabe et al. (U.S. Patent No. 5,481,490); and (b) whether claim 4 is patentable over the combination of Saia et al. in view of Watanabe et al. and further in view of Roy (U.S. Patent No. 6,180,976).

8. GROUPING OF CLAIMS

Although claims 2 – 6 depend from claim 1, none of the claims stand or fall together. Rather, for reasons set forth in the Argument which now follows, it is submitted that each of the claims recites a combination which further distinguishes the invention over the prior art.

9. ARGUMENT

A. A Non-final Rejection of the Claims under Section 103 Was Overcome by Amendment.

In the first office action (mailed 1/28/02) the examiner rejected of all the claims based on combinations of Arai (U.S. Patent No. 5,643,804) with Watanabe and Saia. In the response filed 5/22/02, Claim 1 was amended to successfully distinguish the invention over these combinations. The amendment narrowed the scope of claim 1 from a "semiconductor device" to the specific species of semiconductor devices termed the "monolithic integrated circuit." As explained in the Background, above, the monolithic integrated circuit is by definition a plurality of circuit elements formed on a common body of semiconductor material. Citations have been presented in support of this and there is no information of record which would conflict with this common knowledge that has been in the literature for over 30 years.

The amendment was made because the Arai reference discloses a "composite integrated circuit" or "hybrid integrated circuit" of the type wherein a monolithic integrated circuit is combined with a separate passive component such as a capacitor. With the amendment Applicants more expressly excluded from the claim scope those embodiments wherein an integrated circuit and a separate capacitor may each be mounted on a substrate and connected to one another to form what is termed a hybrid circuit. As a result, applicants' invention is *only* directed to a stack of alternating conductive and insulative layers ***in*** a monolithic integrated circuit. It was also specifically noted in the remarks filed with the 5/22/02 amendment that the claimed "first and second levels of interconnect conductor" are also portions of the monolithic integrated circuit.

Thus applicants have clearly made of record the plain fact that there is no desire to read the pending claims on any structure other than one wherein all of the circuit elements and interconnect conductor are formed on a common semiconductor body, i.e., a monolithic integrated circuit.

By presenting a new rejection in the next office action it appears the examiner agrees with applicants' contention that the Arai reference cannot be combined with the Watanabe reference to meet the terms of claim 1, i.e. a monolithic integrated circuit.

B. Final Rejection of Claim 1 Cannot Stand in View of the Amendment Which Distinguished Over Arai and Watanabe.

In the next office action, mailed 8/26/02, a final rejection of claims 1-3 and 5-6 was imposed based on a new combination of Saia and Wantanabe.

As noted at Col 2, lines 34 – 38, Saia discloses an integral thin film capacitor on a base such as a polymer layer. Saia also discloses a HDI interconnect circuit

module wherein the capacitor of Saia can be applied on a surface of any desired base material including ceramic substrates or printed circuit boards. See Col 2, lines 38 – 44 as well as Figure 5b of Saia. Because Saia's disclosure is applicable to modules, Saia illustrates in Figure 7 a module with "circuit chip 68 having chip pads 77 ... situated in a chip well 70 ..." See Col. 4, lines 54 – 60. It is recognized that the chip 68 of Saia may be a semiconductor integrated circuit.

The final office action states as the basis for rejecting claims 1-3 that

> *"Saia discloses a monolithic integrated circuit (col. 2 lines 24 –27) comprising: a first interconnect level (the level of conductive layer 20); a second interconnect level (the level of a conductive layer 52); a third interconnect level (the level of a conductive layer 58 on an insulating layer 56); a stack of alternating conductive and insulating layers formed in vertical alignment with respect to an underlying plane, wherein the stack layers [sic] formed between the first and second interconnect levels and including a first conductive layer (36), a first insulator layer (38) on the first conductive layer , a second conductive layer (40) on the first insulative layer, a second insulative layer (42) on the second conductive layer, and a third conductive layer (44) on the second insulative layer with the first and third conductive layer commonly connected through the first, second and third interconnect levels. See Saia et al.'s Fig. 7-9.*
>
> *Saia et al. does not explicitly teach that the first and second interconnect levels [sic] to the semiconductor layer.*
>
> *It is well known in the art and also taught by Watanabe et al. that the capacitor structure is commonly connected to a semiconductor layer such as source/drain region of the FET transistor in order to control the charge storage in the capacitor structure by ON/OFF states of the FET transistor.*
>
> *Therefore, it would have been obvious to one of ordinary skill in the art connecting the first and second interconnect levels to semiconductor layer in Saia et al.'s device.*

Essentially, the difference between the first rejection and the final rejection is that the examiner substituted the Saia reference for the Arai reference. Unfortunately, the Saia reference has deficiencies similar to those of the Arai reference. Specifically, the examiner mistakenly urges that Saia discloses a monolithic integrated circuit at column 2, lines 24-27. This is not at all the case. The passage only recites:

"fabricating an integral multi-layer thin film capacitor on a polymer layer using staggered landing pads."

It is also made clear at Column 1 of this reference that Saia deals with high density integrated circuit modules (see lines 1-2) and formation of capacitors on

polymer layers. There is simply no teaching in this reference for the formation of a capacitor structure **in** a monolithic integrated circuit.

To formulate his rejection the examiner had to incorrectly read at least one other of applicant's recitations on Saia. As already noted, applicants require

"at least first and second levels of interconnect conductor for connection to a semiconductor layer ..."

and further require

"a stack of alternating conductive and insulative layers ... between the first and second levels of conductor ..."

To reject the claims the examiner has improperly attempted to read applicant's "second interconnect level" on Saia's capacitor plate 52 by merely referring to the capacitor plate as a "conductive layer". While the capacitor plate is a conductive layer, it is clearly not part of any level of interconnect.

C. The Final Rejection Also Required a Piecemeal Reconstruction of the Prior Art

In presenting this rejection the examiner acknowledges that Saia et al. does not explicitly teach connection of "the first and second interconnect levels to the semiconductor layer" but relies on Watanabe to show that capacitor structures are commonly connected to semiconductor layers. In fact, it is well known that that when capacitor structures are formed in integrated circuits they are connected to semiconductor layers. This is not applicants' invention.

Applicants' invention addresses the need to advance the level of semiconductor process integration by increasing the capacitance on a monolithic semiconductor integrated circuit without increasing the area consumed over a semiconductor region. There is no teaching or suggestion to reconstruct the Saia reference, i.e., to make Saia's module into any monolithic integrated circuit; or by changing Saia's capacitor plate 52 into an interconnect conductor (e.g., a runner) for connection to a semiconductor layer.

Further, it would be improper to combine the references because they teach away from the invention. That is, the examiner merely ignores technical incompatibilities and urges that the "interconnect levels" of Saia could be connected to a semiconductor layer. This is not at all the case.

First, as already noted, it is improper to reconstruct the capacitor plate 52 of Saia as though it were an interconnect conductor. Secondly, the only semiconductor regions that Saia or Watanabe disclose or imply are regions of integrated circuitry such as the source/drain region of a FET (which the examiner has noted from the

Watanabe reference). But, in this regard, Saia clearly teaches away from the examiner's contention.

That is, see Figure 7 and Col. 4, lines 54 – 60 of Saia which specifically teaches connecting the electrical conductor 20 to a chip pad 77 instead of a semiconductor region in the circuit chip 68. It is acknowledged that the circuit chip 68 may be a monolithic integrated circuit. However, it is clear that the "stack" of Saia is not part of the circuit chip 68 or part of any monolithic integrated circuit. Thus Saia's teaching to connect the conductor 20 to the pad 77 in order to make electrical contact with circuit chip 68 is inconsistent with the examiner's speculative and piece meal reconstruction. Clearly it would be improper to substitute a semiconductor layer for a metal contact or other pad such as the pad 77.

It is only the applicants that teach forming the claimed stack "between first and second levels of conductor" and connecting these same conductors to a semiconductor layer with the first and third conductive layers commonly connected.

D. The Dependent Claims 2 – 6 Further Distinguish the Invention Over the Art

The dependent claims do not stand or fall with claim 1. This is because each of the dependent claims includes subject matter which, in combination with other features of the claims, adds additional patentable distinctions.

Claim 2 expressly defines an arrangement for connecting the first and third conductive layers as "through the first and second levels of interconnect conductor."

Claim 3 requires a "third level of interconnect conductor" and an arrangement wherein "the first and second layers [are] commonly connected through the first, second and third levels of interconnect conductor." See, for example, the structure 10 of Figure 1.

Claim 4 presents an additional feature wherein the "conductors connecting the first and third conductive layers include via portions and trench portions ..." The examiner rejects claim 4 further in view of Roy, but Roy does not compensate for the deficiencies already identified in the rejection of claim 1. Rather, a review of Roy confirms that the teachings of the applicants are not known in the prior art of Damascene interconnect structures. Therefore, rejection of claim 4 cannot stand.

Claim 5 requires an arrangement including "one or more pairs of additional conductive and insulative layers formed over the third conductive layer ..." This provides "an uppermost conductive layer commonly connected with the first and third conductive layers."

According to claim 6 the stack of claim 5 "comprises 5 conductive layers configured to provide 4 capacitors connected in parallel. The examiner contends in

the final office action that "Saia et al's device is identical as claimed structure ..." whereas it has already been demonstrated (above) that Saia et al. clearly falls short of meeting the requirements set forth in claim 1.

10. SUMMARY

Based on the foregoing reasons it is apparent that the examiner's rejections are entirely in error and reversal is therefore requested.

Respectfully submitted,

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Date: 21 February 2003

APPENDIX A TO APPEAL BRIEF

For Ser. No. 09/653,295 (Hui 3-6-16)

CLAIMS ON APPEAL

1. (Amended) A monolithic integrated circuit comprising:

at least first and second levels of interconnect conductor for connection to a semiconductor layer; and

a stack of alternating conductive and insulative layers formed in vertical alignment with respect to an underlying plane and formed between the first and second levels of conductor, including

a first conductive layer,

a first insulator layer formed over the first conductive layer,

a second conductive layer formed over the first insulative layer ,

a second insulator layer formed over the second conductive layer, and

a third conductive layer formed over the second insulative layer,

with the first and third conductive layers commonly connected.

2. The device of claim 1 wherein the first and third conductive layers are commonly connected through the first and second levels of interconnect conductor.

3. The device of claim 1 further including a third level of interconnect conductor with the first and second conductor layers commonly connected through the first, second and third levels of interconnect conductor.

4. The device of claim 1 wherein the conductors connecting the first and third conductive layers include via portions and trench portions of a Damascene structure.

5. The device of claim 1 wherein the stack of alternating conductive and insulative layers includes one or more pairs of additional conductive and insulative layers formed over the third conductive layer providing an uppermost conductive layer commonly connected with the first and third conductive layers.

6. The device of claim 5 wherein the stack comprises 5 conductive layers configured to provide 4 capacitors connected in parallel.

ATTACHMENT I TO APPEAL BRIEF

Serial Number 09/653,295

United States Patent Office 3,541,357 Patented Nov. 17, 1970

3,541,357

INTEGRATED CIRCUIT FOR ALTERNATING CURRENT OPERATION

William P. Kram, Fayetteville, N.Y., assignor to General Electric Company, a corporation of New York

Filed Apr. 29, 1968, Ser. No. 724,870
Int. Cl. H03k 3/00
U.S. Cl. 307—303 5 Claims

ABSTRACT OF THE DISCLOSURE

A semiconductor monolithic integrated circuit is provided having reverse biased PN junction substrate isolation, and the circuit is made capable of working directly from an alternating current power supply without disruption of the substrate isolation by provision of an integral switching circuit. The switching circuit is effective to prevent sufficient voltage from developing across the substrate isolation PN junction to cause deleterious forward current across the junction during that portion of the cycle of the alternating current power supply when the substrate isolation PN junction tends to become forward biased.

The present invention relates to improvements in semiconductor integrated circuits of the type having a plurality of circuit elements situated in a common body of semiconductor material and which are sometimes referred to as "monolithic" integrated circuits. More particularly, the present invention relates to improvements in such circuits facilitating operation thereof directly from a supply of alternating current voltage.

In such monolithic integrated circuits, it is a known practice to achieve desired electrical isolation of the various circuit elements, each from its neighbors, by forming them in particular regions or islands in the semiconductor body, each of which islands is electrically separated or isolated from the remaining substrate portion of the semiconductor body by a reverse-biased PN junction. The reverse-bias of this isolating PN junction, or isolation diode as it is sometimes called, is achieved by tying or connecting the substrate to a point of desired potential, or bias-point, in the circuit. The bias-point usually selected is that point which normally has the most extreme potential of opposite polarity from the conductivity type of the substrate, e.g., if the substrate is of P-type conductivity, the bias-point to which it is usually tied is the point having the most negative potential in the circuit. This insures reverse biasing of the isolation diode.

This reverse-biased-junction form of isolation has been found satisfactory in those types of integrated circuits, such as circuits having a direct current or unvarying polarity power supply, wherein the potential of a single selected bias-point never ceases to fulfill the requirement of being the most extreme potential of opposite polarity to the conductivity type of the substrate. However, in some integrated circuits, for example those intended for direct connection to a supply voltage of alternating polarity, some second point in the circuit may periodically have a potential more extreme than the selected bias-point to which the substrate is connected. This causes the normally reverse-biased isolation diode between the substrate and such second point to become forward biased, thereby destroying the desired isolation and producing various undesirable effects such as injection of charge carriers from the substrate across the isolation diode PN junction, and parasitic transistor action between islands or between the substrate and the islands.

One object of the present invention is to provide improvements in reverse-biased-junction isolation integrated circuits which will prevent isolation diodes therein from

becoming deleteriously forward biased when a particular bias-point to which the substrate is tied experiences a potential other than the extreme potential of opposite polarity from the substrate conductivity type.

Another object is to provide improved monolithic integrated circuits particularly suitable for operation in direct connection with an alternating polarity, i.e., alternating current voltage, power supply.

Another object is to provide an improved integrated circuit of the foregoing character which is inexpensive, does not require costly additional process steps to manufacture, and whose use with an alternating current voltage power supply does not require connection of any external auxiliary circuitry.

These and other objects of the invention will be apparent from the following description and the accompanying drawings, wherein:

FIGS. 1 and 2 illustrate one form of semiconductor integrated circuit to which the present invention is applicable;

FIG. 3 is a fragmentary sectional view of a portion of the semiconductor body of the circuit of FIGS. 1 and 2, together with other circuit elements thereof;

FIG. 4 is a schematic diagram of a portion of the circuit of FIG. 3;

FIG. 5 is a circuit similar to that of FIG. 4, modified according to one form of the invention;

FIG. 6 is similar to FIG. 3 and includes the modification of FIG. 5;

FIG. 7 is similar to FIG. 5, modified according to another form of the invention; and

FIG. 8 is similar to FIG. 6, and includes the modification of FIG. 7.

Referring to the drawing, FIGS. 1 and 2 illustrate one form of circuit to which the present invention is applicable. The circuit of FIGS. 1 and 2 includes a half-wave rectifier, connected at terminals 1 and 2 to a power supply S of alternating polarity, and including a capacitor C having one terminal 5 connected to terminal 1 and to the N-region of a diode D1 and the other terminal 3 connected to the P-region of a diode D2. The N-region of diode D2 is connected to terminal 2, as is the P-region of diode D1. Diode D1 may be a so-called avalanche type reverse voltage breakdown diode for limiting the voltage to which capacitor C is allowed to charge. Other circuitry represented by block 4, the details of which constitute no part of the present invention, may be connected in parallel with capacitor C. During the half-cycle of the alternating polarity supply S when terminal 1 is positive and terminal 2 negative, the capacitor C is charged with the polarity shown in FIG. 1 to the voltage level determined by the reverse breakdown voltage of diode D1. During the half-cycle when the polarity of supply S reverses and terminal 1 is negative as shown in FIG. 2, capacitor C is prevented from discharging back into the supply S by diode D2.

All of the circuit elements thus far described, except the alternating supply S and capacitor C, may be constituted by a monolithic integrated circuit, the outline of the semiconductor body of which is illustrated by the dotted line 6 in FIGS. 1 and 2. A sectional view of a portion of the semiconductor body 6 of the integrated circuit of FIGS. 1 and 2 is shown in FIG. 3, omitting for simplicity and ease of understanding, all the normal junction-covering and protective insulative layers whose composition and function is well understood by those skilled in the art. The substrate portion of the semiconductor body 6 is shown at 20, and may, for example, be of P-type conductivity. Substrate portion 20 surrounds respective islands defined by isolating PN junctions 21 and 22, and diodes D1 and D2 are formed as shown

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The present invention relates to improvements in semiconductor integrated circuits of the type having a plurality of circuit elements situated in a common body of semiconductor material and which are sometimes referred to as "monolithic" integrated circuits. More particularly, the present invention relates to improvements in such circuits facilitating operation thereof directly from a supply of alternating current voltage.

In such monolithic integrated circuits, it is a known practice to achieve desired electrical isolation of the various circuit elements, each from its neighbors, by forming them in particular regions or islands in the semiconductor body, each of which islands is electrically separated or isolated from the remaining substrate portion of the semiconductor body by a reverse-biased PN junction. The reverse-bias of this isolating PN junction, or isolation diode as it is sometimes called, is achieved by tying or connecting the substrate to a point of desired potential, or bias-point, in the circuit. The bias-point usually selected is that point which normally has the most extreme potential of opposite polarity from the conductivity type of the substrate, e.g., if the substrate is of P-type conductivity, the bias-point to which it is usually tied is the point having the most negative potential in the circuit. This insures reverse biasing of the isolation diode.

This reverse-biased-junction form of isolation has been found satisfactory in those types of integrated circuits, such as circuits having a direct current or unvarying polarity power supply, wherein the potential of a single selected bias-point never ceases to fulfill the requirement of being the most extreme potential of opposite polarity to the conductivity type of the substrate. However, in some integrated circuits, for example those intended for direct connection to a supply voltage of alternating polarity, some second point in the circuit may periodically have a potential more extreme than the selected bias-point to which the substrate is connected. This causes the normally reverse-biased isolation diode between the substrate and such second point to become forward biased, thereby destroying the desired isolation and producing various undesirable effects such as injection of charge carriers from the substrate across the isolation diode PN junction, and parasitic transistor action between islands or between the substrate and the islands.

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becoming deleteriously forward biased when a particular bias-point to which the substrate is tied experiences a potential other than the extreme potential of opposite polarity from the substrate conductivity type.

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INTEGRATED CIRCUIT FOR ALTERNATING CURRENT OPERATION

Filed April 29, 1968 2 Sheets-Sheet 2

FIG.6.

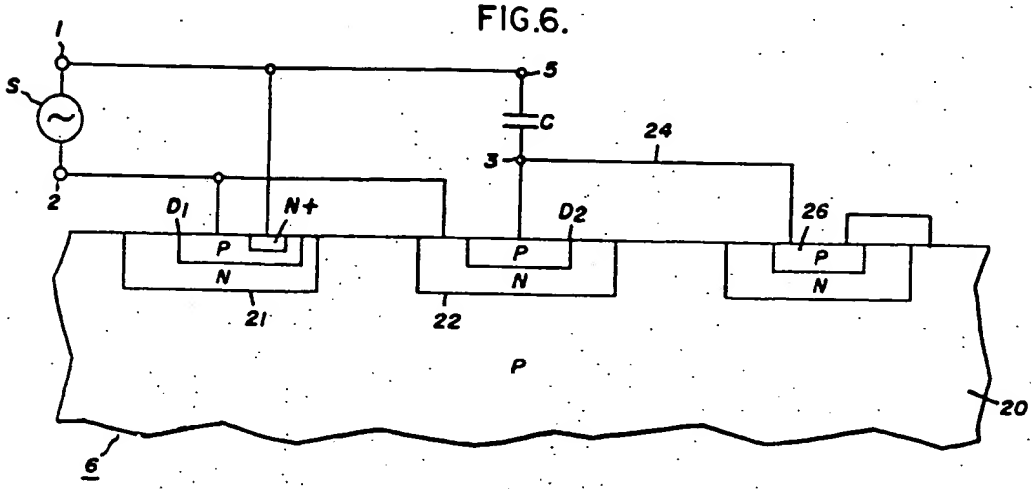


FIG.7.

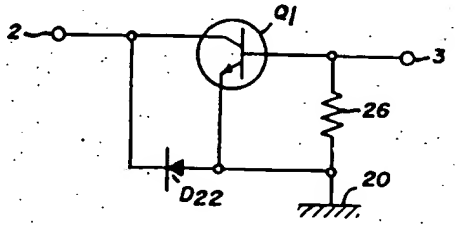
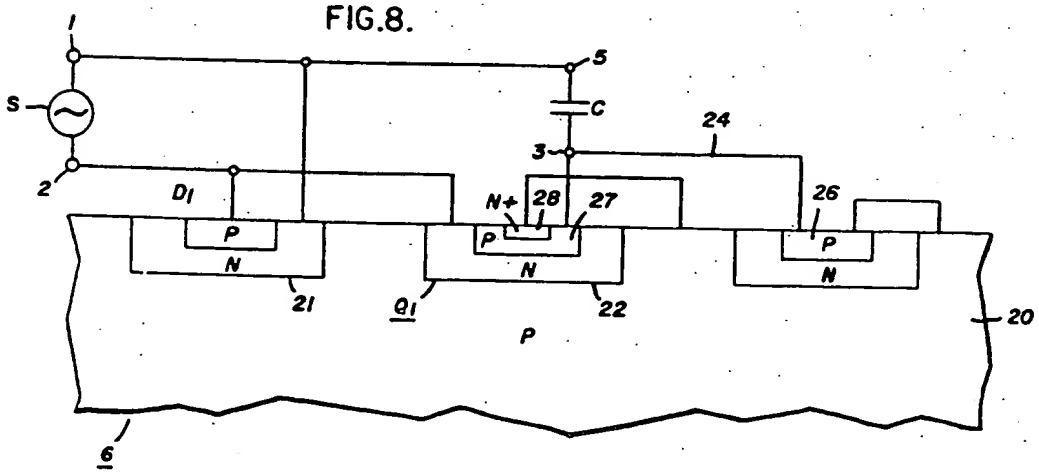


FIG.8.



INVENTOR:
WILLIAM P. KRAM,
BY Robert J. Mooney
HIS ATTORNEY.

Nov. 17, 1970 W. P. KRAM 3,541,357

INTEGRATED CIRCUIT FOR ALTERNATING CURRENT OPERATION

Filed April 29, 1968 2 Sheets-Sheet 1

FIG.1.

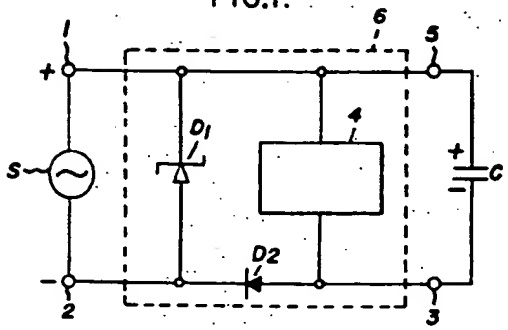


FIG.2.

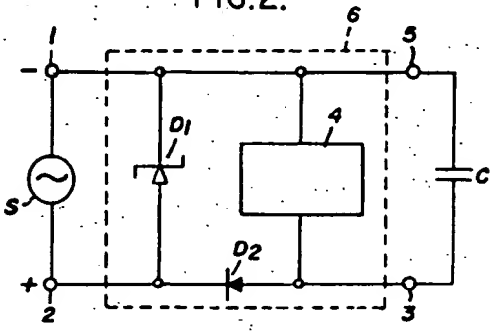


FIG.3.

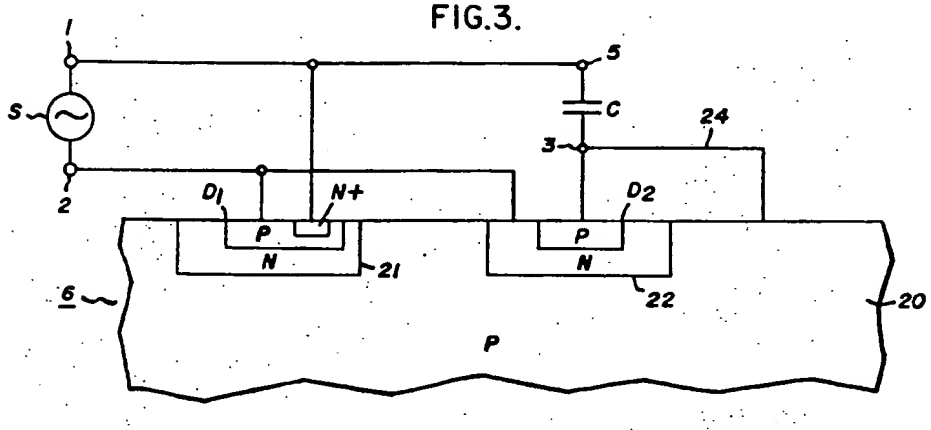


FIG.4.

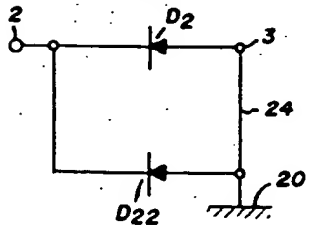
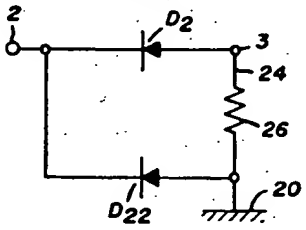


FIG.5.



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HIS ATTORNEY.

Nov. 17, 1970 W. P. KRAM 3,541,357

INTEGRATED CIRCUIT FOR ALTERNATING CURRENT OPERATION

Filed April 29, 1968 2 Sheets-Sheet 1

FIG.1.

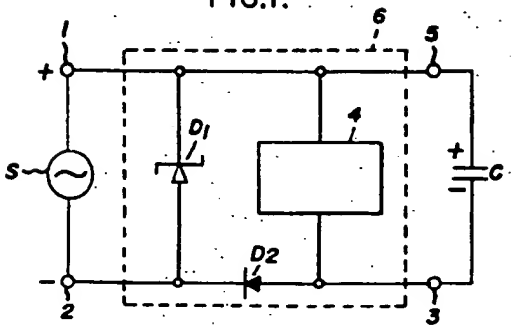


FIG.2.

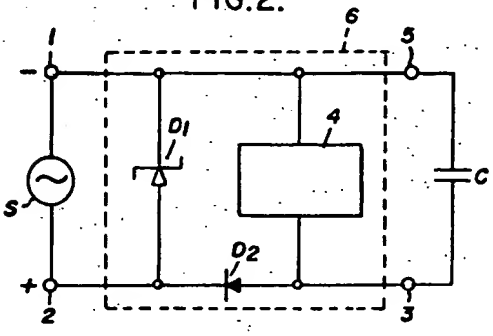


FIG.3.

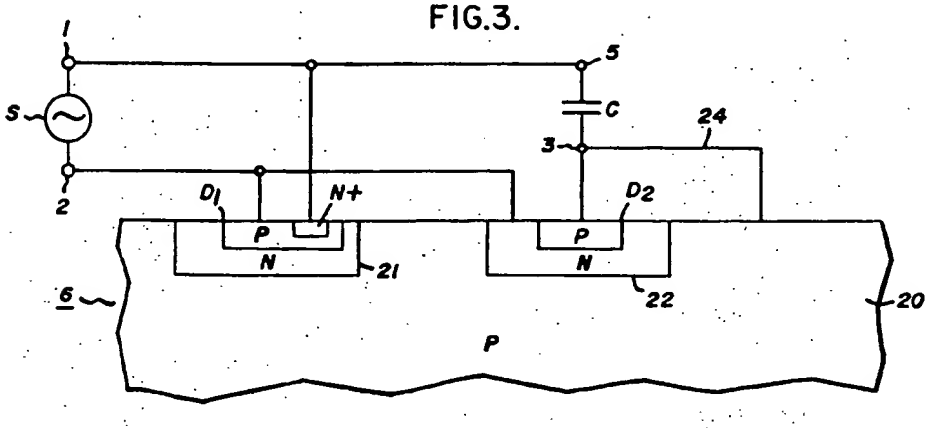


FIG.4.

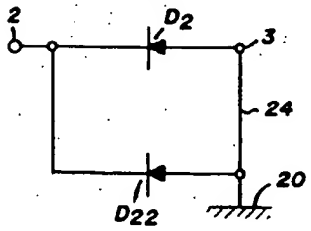
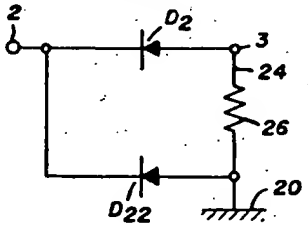


FIG.5.



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INTEGRATED CIRCUIT FOR ALTERNATING CURRENT OPERATION

Filed April 29, 1968 2 Sheets-Sheet 1

FIG.1.

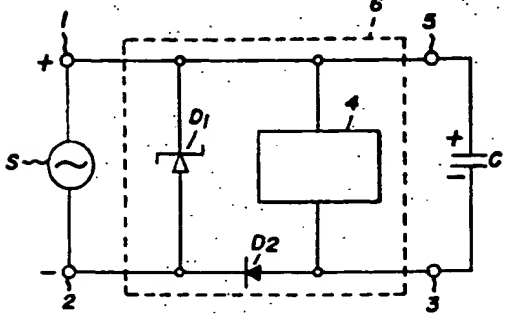


FIG.2.

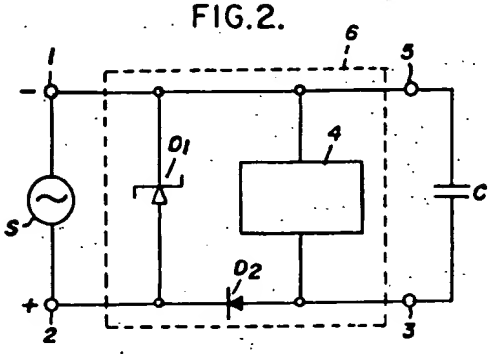


FIG.3.

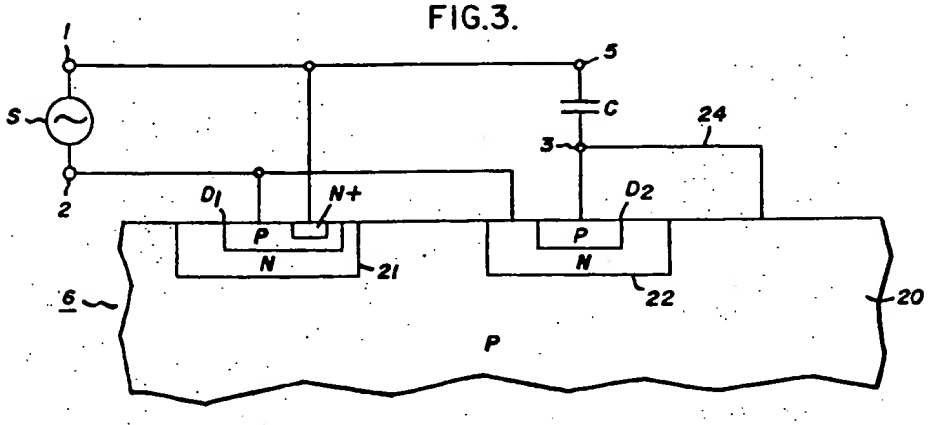


FIG.4.

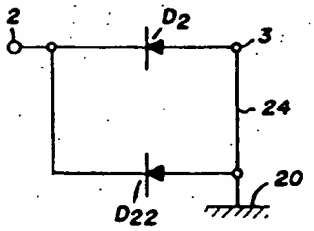
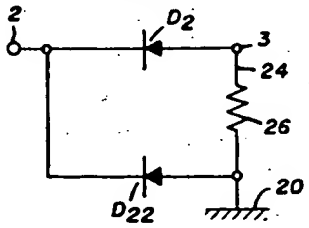


FIG.5.



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within these islands. Junctions 21 and 22, therefore, constitute isolating diodes which should be reverse biased to properly electrically isolate the islands from each other and isolate the substrate 20 from the remainder of the structure.

FIG. 4 shows schematically that portion of the circuit of FIG. 3 include diode D2, the substrate 20, and the isolating diode D22 formed by the substrate-isolating junction 22. As will be evident from FIG. 4, the substrate 20 is connected to terminal 2 through the isolating diode D22, and is connected directly to terminal 3 by conductor 24.

In the operation of the circuit of FIGS. 1 through 4, when terminal 1 is positive, the capacitor C is charged as shown in FIG. 1 and the most negative point in the circuit, i.e., the point of most extreme potential of polarity opposite to that of the P-type substrate 20, is terminal 2. When terminal 2 becomes positive, diode D1 conducts in the forward direction, diode D2 prevents the capacitor C from completely discharging and the most negative point in the circuit shifts to terminal 3. Thus, if the substrate 20 is tied, as indicated by conductor 24, to terminal 3 as a normal bias-point, junctions 21 and 22 of FIG. 3 will be reverse biased for proper isolating during the half cycle when terminal 2 is positive. But during the half cycle when terminal 1 is positive and terminal 2 becomes more negative than terminal 3, junction 22 will become temporarily forward baised and substrate 20 will become connected by a low impedance path to terminal 2, and those portions of the circuit likewise connected to terminal 2, through the forward-biased junction 22. Obviously this would completely disrupt the desired isolation and produce a variety of deleterious effects on circuit performance.

To prevent junction 22 from becoming forward biased when terminal 2 becomes more negative than terminal 3, the present invention provides for clamping the substrate 20 to whatever portion of the circuit has the most extreme potential of the opposite polarity from the conductivity type of the substrate, i.e., the most negative-going portion of the P-type substrate circuit of FIG. 3. So that when the potential of terminal 2 becomes more extreme, i.e., more negative than that of terminal 3, the potential of substrate 20 is according to the present invention correspondingly made more negative.

FIG. 5 is similar to FIG. 4 but shows how forward biasing of substrate diode D22 is effectively minimized according to one form of the present invention. Basically, the present invention provides means for reducing the current flow through the substrate diode D22, when the substrate diode tends to become forward biased, to a level such that carrier injection at the substrate diode is insufficient to cause harmful parasitic effects in the circuit. This is accomplished by preventing forward voltage across the substrate diode D22 from exceeding that value, e.g., approximately 0.3 volt in the case of a substrate of germanium semiconductor material and 0.6 volt in the case of silicon, where the well-known "knee" occurs in the graph of forward current vs. forward voltage for such diodes. Such "knee" is shown for example in FIG. 1.17 of the General Electric Transistor Manual, 7th edition, copyright 1964.

In the circuit of FIG. 5, forward biasing of diode D22 is effectively minimized by placing a resistor 26 in the path 24 between substrate 20 and terminal 3. The resistor 26 is thus in series with diode D22, with relation to the path between terminal 3 and terminal 2, and is of a value sufficiently large to reduce the voltage across diode D22, and the current through diode D22, below a level so that carrier injection across the PN junction of diode D22 is insufficient to cause harmful parasitic effects in the circuit or degrade the isolation of other elements of the circuit from each other and from the substrate. The value of resistor 26 should be sufficiently large to limit the forward voltage drop across diode D22 in accordance with

the above-defined criteria, e.g., to less than about 0.6 volt in the case of silicon, but should not be so large as to allow the substrate to in effect be disconnected from terminal 3, during the half cycle of the AC supply when terminal 3 is the most extreme potential point in the circuit. Thus the optimum value of resistor 26 will depend somewhat on current levels in the particular circuit to which the invention is applied, but it has been found that a resistance value of about 100–5,000 ohms is normally sufficient for resistor 26 when silicon is the integrated circuit semiconductor material.

In the circuit of FIG. 5, the diode D2 should, for optimum effect in limiting forward voltage drop across diode D22, have as low as possible a forward voltage drop of its own. Accordingly, diode D2 may preferably be of a type having an inherently low forward voltage drop, such as a Schottky diode.

FIG. 6 shows the semiconductor body 6 of FIG. 3 modified to include resistor 26 in the connective path between terminal 3 and substrate 20. The resistor 26 may, as is well understood by those skilled in the art, be provided in the physical or structural form of an impurity impregnated region within body 6 produced by conventional diffusion processes simultaneously with the formation of diodes D1 and D2, thereby essentially precluding any extra costs or process steps in the provision of resistor 26. As is shown in FIG. 6, resistor 26 is thereby formed within an island 26A which separates resistor 26 from substrate 20.

Another form of the invention is shown in FIGS. 7 and 8. FIG. 7 is similar to FIG. 6 except that diode D2 is replaced by an NPN transistor Q1, the base of which is tied to terminal 3, the collector to terminal 2, and the emitter to substrate 20. In the operation of the circuit of FIGS. 7 and 8, when the potential at terminal 2 becomes more negative than that at terminal 3, transistor Q1 conducts and shunts isolation diode D22, clamping substrate 20 to terminal 2 and preventing D22 from becoming forward biased.

The transistor circuit embodiment of FIG. 7 is preferred to the diode circuit embodiment of FIG. 5 because the collector-emitter voltage drop of a conducting transistor is usually less than the forward voltage drop of a diode, so the transistor Q1 provides a more effective shunt for diode D22 to insure that D22 will not become forward biased during circuit operation.

Although the transistor Q1 can be arranged with either emitter or collector connected to substrate 20, the inverse mode of connection, i.e., with collector of Q1 connected to terminal 2 and emitter of Q1 connected to substrate 20, is preferred to the normal mode because the higher reverse voltage capability of the collector-base junction of the transistor is then available in the circuit between terminals 2 and 3 when the transistor is not turned on.

FIG. 8 is similar to FIGS. 3 and 6 and shows the semiconductor body of FIG. 3 modified to include transistor Q1 in place of diode D2. The base region 27 of transistor Q1 may, of course, be formed by conventional diffusion process steps simultaneously with the formation of diode D1 and resistor 26, or simultaneously with formation of other circuit elements, and the emitter region 28 may be likewise formed simultaneously with other circuit elements so that essentially no additional process steps or processing costs are required to include transistor Q1 in the circuit.

It will be appreciated by those skilled in the art that the invention may be carried out in various ways and may take various forms and embodiments other than the illustrative embodiments heretofore described. Accordingly, it is to be understood that the scope of the invention is not limited by the details of the foregoing description, but will be defined in the following claims.

What I claim as new and desire to secure by Letters Patent of the United States is:

1. In a monolithic semiconductor integrated circuit

adapted to be energized by a power supply of alternating polarity and including a body of semiconductor material having a region forming a circuit element isolated from a substrate portion of the body by a PN junction diode formed between said circuit element and said substrate portion, a first bias point in said circuit having, when said power supply has one polarity, a potential more extreme than that of said region and of polarity opposite to the conductivity type of said substrate portion, means for reverse-biasing said PN junction when said power supply has said one polarity comprising first connector means extending between said substrate portion and said first bias point, a second bias point in said circuit having, when said power supply has a polarity opposite to said one polarity, a potential more extreme than that of said region and of polarity opposite to the conductivity type of said substrate portion, and means for preventing said PN junction diode from becoming forward biased sufficiently to permit deleterious flow of charge carriers thereacross when said power supply alternates to said opposite polarity comprising second connector means in circuit with said substrate and said second bias point for clamping said substrate at a potential differing from the potential of said second bias point by an amount less than the voltage at the knee of the forward conduction voltage-current curve of said PN junction diode.

2. The circuit defined in claim 1 wherein said second connector means includes a transistor having its base tied to said first bias point, one of the other electrodes of the transistor being tied to the substrate portion of the body, and the other of the electrodes of the transistor being tied to the second bias point.

3. The circuit defined in claim 1 wherein said second connector means includes a transistor having its base tied to said first bias point, the normal collector of the transistor being connected in inverse mode as an emitter to said second bias point, and the normal emitter of said transistor being connected in inverse mode as a collector to said substrate portion of the body.

4. The circuit defined in claim 1 wherein said second connector means includes a resistor connected between said substrate and said first bias point.

5. In a monolithic semiconductor integrated circuit adapted to be energized by a power supply of alternating polarity and including a body of semiconductor material having a region forming a circuit element isolated from a substrate portion of the body by a PN junction diode formed between said circuit element and said substrate portion, a first bias point in said circuit having, when said power supply has one polarity, a potential more extreme than that of said region and of polarity opposite to the conductivity type of said substrate portion, means for reverse-biasing said PN junction when said power supply has said one polarity comprising first connector means extending between said substrate portion and said first bias point, a second bias point in said circuit having, when said power supply has a polarity opposite to said one polarity, a potential more extreme than that of said region and of polarity opposite to the conductivity type of said substrate portion, and switching circuit means providing a low impedance connection between said substrate and said second bias point whenever said power supply has said opposite polarity to prevent said PN junction diode from becoming deleteriously forward biased.

References Cited

UNITED STATES PATENTS

3,230,429	1/1966	Stehney	307—303 X
3,421,025	1/1969	Mitchell et al.	307—303 X

DONALD D. FORRER, Primary Examiner

R. C. WOODBRIDGE, Assistant Examiner

U.S. Cl. X.R.

307—237; 317—235

ATTACHMENT II
TO APPEAL BRIEF
Serial Number 09/653,295

United States Patent **4,245,231**
Davies **January 13, 1981**

Combination capacitor and transistor structure for use in monolithic circuits

Abstract

A combination capacitor and transistor structure is described wherein the capacitor is formed integrally with the emitter electrode of the transistor. The transistor is formed in a ***monolithic integrated circuit*** using generally known techniques and constitutes a vertically integrated PNP device. The emitter electrode of the transistor which comprises a P+ diffusion region is of a predetermined area which is large enough to form the bottom plate of the capacitor. The top plate of the capacitor is formed by growing a dielectric material over the diffused emitter region and then forming metallization thereover. The combination capacitor and transistor structure may be utilized in a bias network for biasing the output stage of an operational amplifier in a class AB mode. The capacitor formed in the combination structure may be utilized as the compensation capacitor in such operational amplifier which utilizes pole splitting techniques. The improvement provided by the invention reduces the surface area of the semiconductor die chip required to form the capacitor and transistor which facilitates greater device density on a particular die chip.

Inventors: **Davies; Robert B.** (Tempe, AZ)
Assignee: **Motorola Inc.** (Schaumburg, IL)
Appl. No.: **973407**
Filed: **December 26, 1978**

Current U.S. Class: **257/296**; 257/532; 257/566; 257/E27.042
Intern'l Class: H01L 027/02
Field of Search: 357/51,48,52,55

References Cited [Referenced By]

U.S. Patent Documents

3953875	Apr., 1976	Cave et al.	357/51.

Primary Examiner: Wojciechowicz; Edward J.
Attorney, Agent or Firm: Bingham; Michael D.

Claims

What is claimed is:

1. In a monolithic integrated circuit having a substrate region of semiconductor material of a first conductivity type, an epitaxial region of semiconductor material of a second conductivity type formed on the substrate region, a portion of the epitaxial region being isolated by an isolation region of semiconductor material of the first conductive type from the remainder thereof wherein an isolation pocket of the epitaxial region is defined, a combination capacitor and transistor structure, the improvement comprising:

the isolated epitaxial pocket region having an outwardly planar facing surface and being the base region of the transistor, the substrate region lying under the isolated epitaxial pocket region being the collector region of the transistor;

a first defined region of semiconductor material of the first conductivity type formed in the isolated epitaxial pocket region and having an outwardly facing surface coplanar with said outwardly facing surface of said isolated epitaxial pocket region, said first region being the emitter region of the transistor;

a layer of dielectric material formed over said first region;

a layer of metallic material formed over the dielectric material and said first region; and

said layer of metallic material, in combination with said dielectric material and said first region forming a capacitor with said metallic material being a first plate of the capacitor and the active emitter region of the transistor being a second plate of the capacitor wherein the combined capacitor and transistor structure is realized by the capacitor being formed integrally with the active emitter region of the transistor.

2. The monolithic integrated circuit of claim 3 wherein said substrate region is of a P conductivity type, said first region is of said N- conductivity type, and said second and third regions are of said P+ conductivity type.

3. The monolithic integrated circuit of claim 1 including:

a second defined region of semiconductor material of said first conductivity type formed in the isolated epitaxial pocket region in spaced relationship to said first region, said second region having an outwardly facing surface and forming with the substrate region and the isolated epitaxial pocket region a second transistor of the same conductivity type as the transistor of the combination transistor and capacitor structure.

Description

BACKGROUND OF THE INVENTION

This invention relates to operational amplifiers operated in class AB mode and more particularly to a combination capacitor structure and transistor circuit for providing bias to the output stages of the operational amplifiers for facilitating class AB modes of operation.

Contemporary high performance operational amplifiers generally are operated in a class AB mode and comprise a cascaded output section including an NPN and PNP output transistors. The PNP output transistor is usually coupled to a bias circuit which biases the transistor in a class AB mode of operation. Thus, the amplifier is characterized by low current drain and good fidelity. Examples of high performance operational amplifiers which may be operated in class AB modes are the MC1458 and MC1741 operational amplifiers manufactured by Motorola, Inc. These operational amplifiers use a compensation capacitor and pole splitting techniques to set the transfer characteristics of the amplifiers. The compensation capacitor is typically anywhere from 5-30 picofarads and is constructed integrally with the monolithic integrated operational amplifier. In these operational amplifiers substantial semiconductor die real estate is required for the capacitor which may be a disproportionate portion of the total semiconductor area required for the circuit. Furthermore, contemporary operational amplifiers usually utilize an NPN device for biasing the PNP output device in a class AB mode. This creates an inherent mismatch between the two devices which may require more current drain through the output stage than desirable and with less predictable currents being defined which in turn affects the operation of the operational amplifier.

In the design of high performance operational amplifiers it is very desirable to reduce the current drain through the output stages as much as possible to reduce the amount of total drain current required by the amplifier. However, even though the goal is to reduce the current drain in the output stage, it is also important that predictable currents be obtained. Moreover, as the tendancy is to make integrated circuits more complex, it is significant to be able to reduce the die surface area which is required to fabricate an operating circuit.

In view of the above, a need exists for providing a bias circuit for high performance operational amplifiers which can reduce the current drain through the output stage as well as reducing the die surface area required for fabricating the operational amplifier circuit.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a combination capacitor and transistor structure for facilitating class AB bias to the output stage of an operational amplifier while minimizing integrated circuit chip area required for said combination.

The invention relates to a combination capacitor and transistor structure for use in a bias circuit. The combination capacitor and transistor structure includes a transistor having its emitter electrode integrally formed as a bottom plate of the capacitor and its base electrode coupled to a node which may be connected to an output device in an output stage of an operational amplifier which is required to be biased in a class AB mode of operation. The transistor may be part of a bias network which establishes the class AB bias to the output device.

The transistor structure is formed using general vertical bipolar techniques wherein a substrate material of a first conductivity type is used with an epitaxial region of a second conductivity type formed on said substrate region and having an outwardly facing surface. A second region of said first conductivity type is formed in said epitaxial region which has an outwardly facing surface substantially coplanar with said surface of said epitaxial region with said second region having a predetermined surface area which forms both the emitter diffused region of the transistor and the bottom plate of the capacitor structure. A layer of dielectric material is formed over the emitter diffused or second region area which has a layer of

metallization formed thereover to form the top plate of the capacitor. Thus, as described, there is formed a capacitor in series with the emitter electrode of the transistor wherein the combination structure can be utilized in a biasing network for biasing the output stage of generally known operation amplifiers in a class AB mode of operation without requiring mutually exclusive semiconductor die areas for formation of the aforesaid transistor and capacitor.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a combination capacitor and transistor structure of the embodiment of the invention which is suitable for fabrication in monolithic integrated circuit form; and

FIG. 2 is a cross-sectional view of a semiconductor die illustrating the embodiment of the capacitor and transistor structure of FIG. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 is a schematic diagram illustrating the embodiment of the present invention. More specifically, in a practical application the invention may be utilized in an operational amplifier which is operated in a class AB mode. An example of an operational amplifier in which the invention may be utilized is the MC1458 and MC1741 monolithic amplifiers which are two of a group of operational amplifiers manufactured by Motorola, Inc.

The circuit shown by reference numeral 10 would form part of the class AB bias circuitry which is utilized to bias the cascaded output stage of the aforementioned operational amplifiers. For example, PNP transistor 12 would be one of the output cascaded devices of the output stage of the amplifier having its emitter connected to node 14 which would be the output of the operational amplifier. Coupled in cascade with the output node 14 would be an NPN output device. The collector electrode of transistor 12 is connected to node 16 at which may be supplied a source of negative potential or, if desired, a ground reference potential.

PNP transistor 18 which in combination with compensation capacitor 20 comprise the combination structure of the invention may be included in the aforedescribed bias network for biasing the operational amplifier in a class AB mode. Compensation capacitor 20 provides the dominate pole of the transfer function of the operational amplifier and set the first break point, as is known. As shown, one plate of capacitor 20 is connected to node 22 which may be coupled to an input stage if the combination structure is used in an operational amplifier circuit. The other plate of capacitor 20 is integrally formed with the emitter electrode of transistor 18 to constitute the invention. The base electrode of transistor 18 is integrally connected to the base electrode of transistor 12 at node 24.

Transistor 18, if utilized in the bias circuitry for setting the AB bias for output device 12, is usually shown in the prior art as an NPN device. However, by using a PNP device the characteristics of transistor 18 can be matched to that of the PNP output device transistor 12 for better circuit operation. Generally, it is desirable to have the currents through transistor 12 and 18 well defined. Moreover, as transistor 18 sets the AB bias conditions for transistor 12 it is desirable to have the magnitude of the voltage at node 26 larger than the value of the voltage at node 14 while maintaining current drain through the output stage of the operational amplifier (including transistor 12) at a minimum.

By area rationing the emitter areas of transistors 12 and 18 with respect to each other wherein the emitter area of transistor 18 is N times larger than emitter area of transistor 12 the above goals can be met. Thus, a defined current is maintained through transistor 18 to define a smaller quiescent operating current through transistor 12.

At the same time it may be shown that the utilization of a larger emitter area for transistor 12 permits the combination therewith of the required compensation capacitor 20. Hence, the use of a PNP transistor as a portion of the biasing circuit for operating the operational amplifier in a class AB mode allows the novel combination structure shown in FIG. 1.

The advantage of the aforedescribed combination capacitor and transistor structure is that no increase in semiconductor die area is required since the increased emitter area provides the bottom plate of capacitor 20. Therefore, a reduction in die area may be realized by the aforedescribed combination. This reduction in semiconductor die area becomes significant when it is considered that the combination capacitor and transistor structure may be utilized in an operational amplifier wherein the operational amplifier is either a dual or quad type operational amplifier where multi-operational amplifiers are fabricated on one semiconductor monolithic integrated chip.

Turning to FIG. 2 there is shown a cross-sectional view of the circuit structure shown in FIG. 1. The structure includes a P-type substrate 28 which comprises the collector electrodes of transistors 12 and 18. A layer of N-type epitaxial semiconductor material 30 is provided over substrate 28 and has an outwardly facing surface. The growth of the epitaxial semiconductor material over substrate 28 utilizes well known fabrication techniques. Further, using known monolithic photolithographic techniques, P+ isolated regions 32, as well as P+ emitter regions 34 and 36 are diffused into epitaxial region 30. As shown, the area of emitter diffused region 34 which comprises the emitter electrode of transistor 18 is larger than the emitter diffused region 36 which forms the emitter electrode of transistor 12. Additionally, N+ regions 38 are diffused into epitaxial region 30. Next, a layer of dielectric material 40 is placed or formed over the surface of the resulting semiconductor structure and openings are selectively provided using photoetching techniques. Then, a layer of metallization is applied over the dielectric material 40 and selectively patterned to provide different contacts. For example, metallization layer 42 which is spaced over a portion of the emitter diffused region of transistor 18 provides the top plate of capacitor 20. The bottom plate of capacitor 20 is formed by the emitter diffused region 34. Metallization contacts 44, 46 and 48 provide contact means with the electrode of transistor 18, the interconnected base electrodes of transistors 12 and 18, and the emitter electrode of transistor 12 respectively. Thus, as shown the combination capacitor structure and transistor 20 and 18 are integrally formed utilizing the emitter diffusion region for the transistor. Thus, a separate portion of the semiconductor chip surface area is not required to form capacitor 20 and transistor 18.

What has been described, therefore, is an improved monolithic integrated circuit comprising a combination capacitor and transistor structure. This combination structure may be utilized in the bias circuitry of monolithic integrated operational amplifiers to bias the output stage of such operational amplifiers in a class AB mode. Since the capacitor structure is formed integrally and overlies an otherwise necessary emitter diffusion region the capacitor structure takes up virtually no additional surface area on the integrated circuit chip. Therefore, more integrated circuits can be provided per wafer than if other types of capacitor structures were utilized.

* * * * *

ATTACHMENT III
TO APPEAL BRIEF
Serial Number 09/653,295

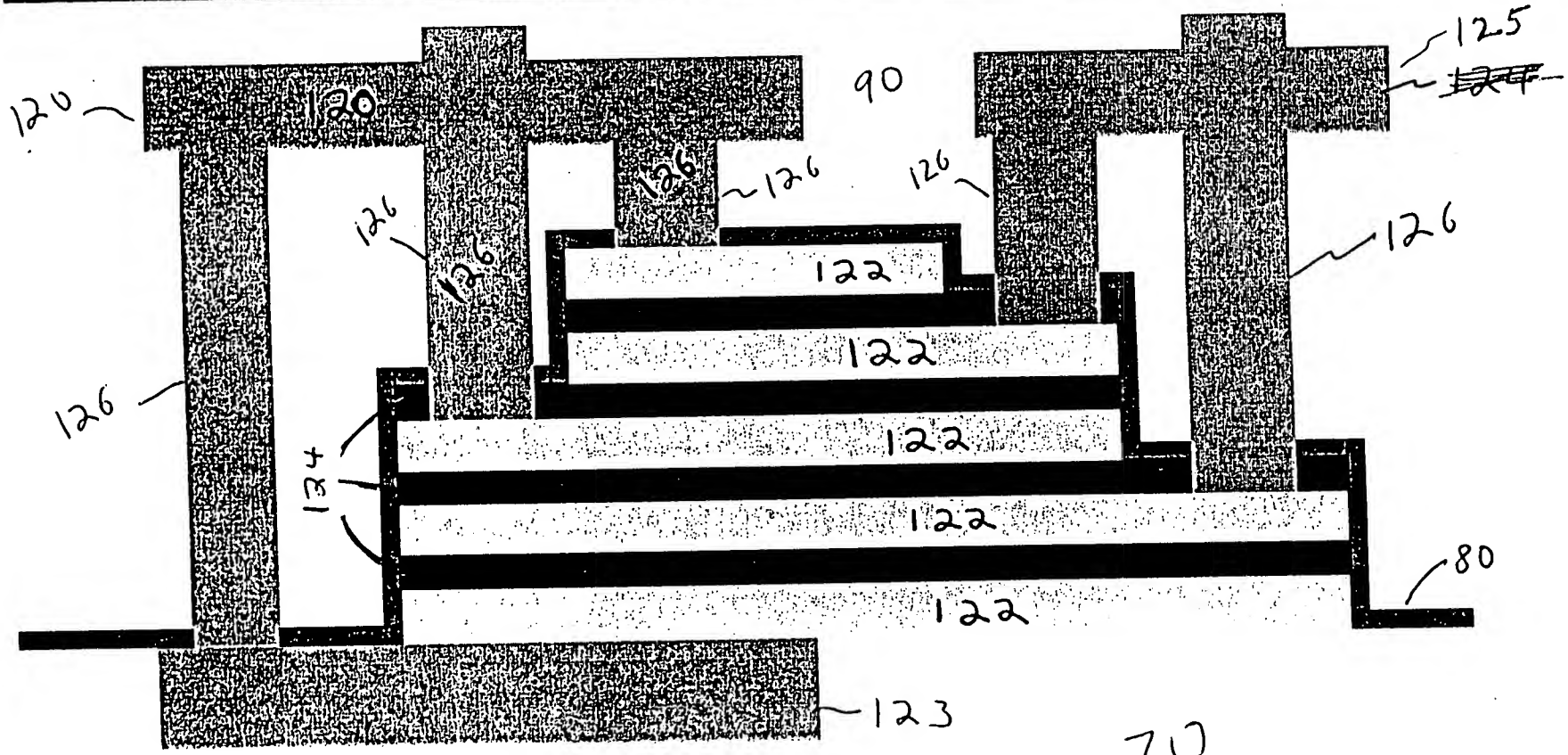

FIGURE 9

Lucent Technologies
Bell Labs Innovations

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

CASE Hui

Serial No. 09/653,295 **Group Art Unit** 2815

Filed August 31, 2000

Examiner Nguyen

Title **Stacked Structure For Parallel Capacitors And Method Of Fabrication**

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Enclosed is an Appeal Brief in the above-identified application.

Please charge the amount of **$330.00** to **Agere Systems Deposit Account No. 501735** to cover the fee. Duplicate copies of this letter are enclosed.

In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 501735** as required to correct the error.

Respectfully,

Ferdinand M. Romano

Ferdinand M. Romano, Attorney
Reg. No. 32752
407-371-3250.

Date: 21 February 2003

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